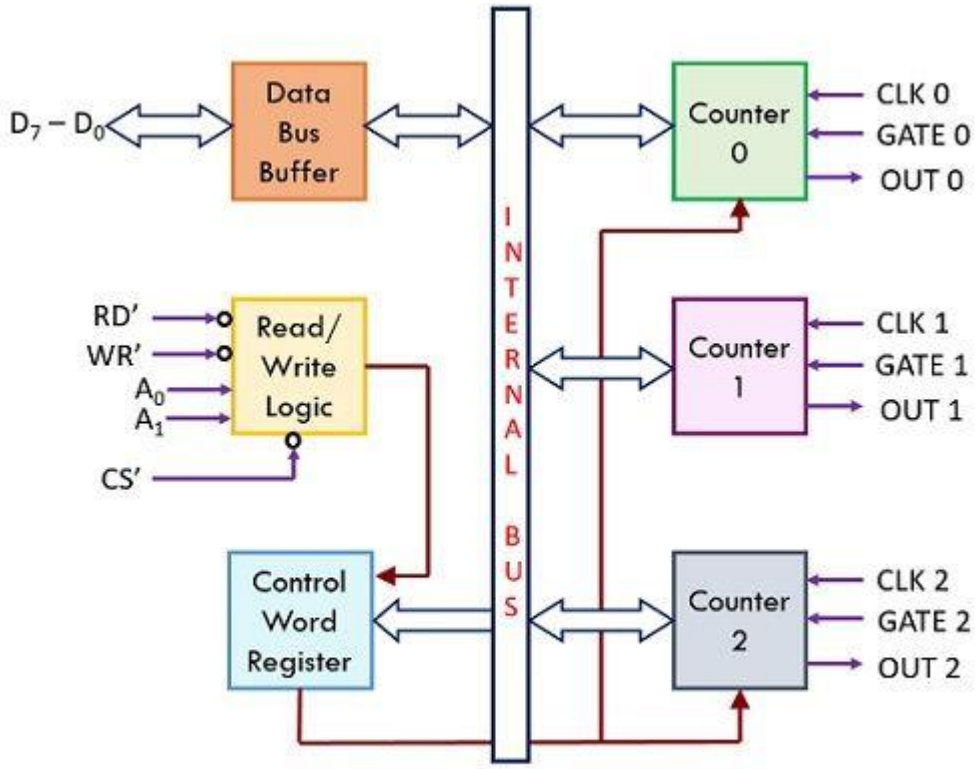
8254 PROGRAMMABLE INTERVAL TIMER

8254 is a device designed to solve the timing control problems in a microprocessor. It has 3 independent counters, each capable of handling clock inputs up to 10 MHz, and size of each counter is 16 bit. It operates in +5V regulated power supply and has 24 pin signals. All modes are software programmable. The 8254 is an advanced version of 8253 which did not offered the feature of read back command.

8254 ARCHITECTURE



Functional Block Diagram of 8254 Timer

The 8-bit bidirectional data buffer interfaces internal circuit of 825 to microprocessor system bus. Data is transmitted or received by the buffer upon the execution of IN or Out instruction. The read/write logic controls the direction of the data buffer depending upon whether it is a read or a write operation. It may be noted that IN instruction reads data while OUT instruction writes data to a peripheral.

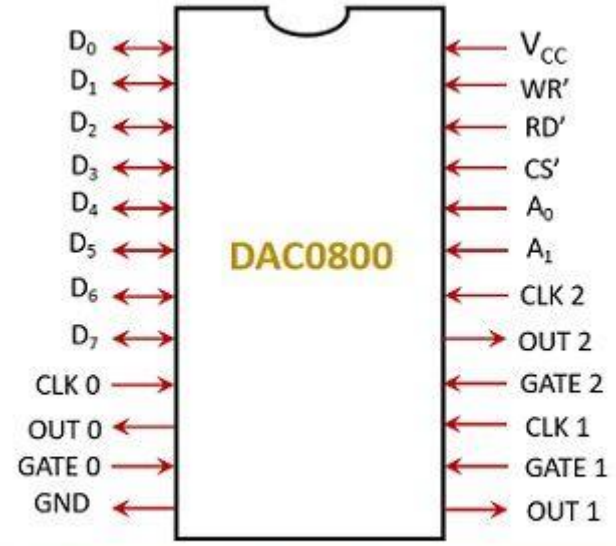
- It includes three 16-bit counters that can work independently in 6
- different modes.
- It is packaged in a 24-pin DIP(Dual in-line package) and requires +5V power supply.
- It can count either in binary or BCD.
- It's counters can operate at a maximum frequency of 10 MHz.

A0 and A1 pins are address input pins ans are required internally for addressing the mode control word register and the three counter registers.A low on CS line enables the 8254 .N operation will be performed by 8254 till it is enabled .

Selected Operations for Various Control Inputs of 8254

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	*Selected Operation*
0	1	0	0	0	Write Counter 0
0	1	0	0	1	Write Counter 1
0	1	0	1	0	Write Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No Operation (tristated)
0	1	1	×	×	No Operation (tristated)
1	×	×	×	×	Disabled (tristated)

Signal description of 8254



Pin Diagram of 8254

A0, A1: The address inputs select one of the four internal registers within the 8254.

A1	A0	Function
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word

CS: Chip select enables the 8254 for programming and for reading or writing a counter.

Vcc: Power connects to the +5V power supply.

GND: Ground connects to the system ground bus.

GATE : The gate input controls the operation of the counter in some modes of operation.

GATE 0	Gate input of counter 0
GATE 1	Gate input of counter 1
GATE 2	Gate input of counter 2

D0-D7: Bidirectional three state data bus lines connected to system data bus.

CLK : The clock input is the timing source for each of the internal counters. This input is often connected to the PCLK signal from the microprocessor system bus controller.

CLK0	Clock input of counter 0
CLK1	Clock input of counter 1
CLK2	Clock input of counter 2

OUT: A counter output is where the waveform generated by the counter is available.

OUT 0	Output of counter 0
OUT 1	Output of counter 1
OUT 2	Output of counter 2

$\overline{\boldsymbol{RD}}$: Read causes data to be read from the 8254 and often connected to the $\overline{IORC}$ signal.

$\overline{\boldsymbol{WR}}$: Write causes data to be written to the 8254 and often connects to the write strobe ($\overline{IOWC}$)

Control Word Register

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Control Word Format

SC_1	SC_0	OPERATION
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

SC-Select Counter Bit Definitions

RL_1	RL_0	OPERATION
0	0	Latch Counter for 'ON THE FLY' reading
0	1	Read/Load Least Significant Byte only
1	0	Read/Load MSB only
1	1	Read/Load LSB first then MSB

RL-Read/Load Bit Definitions

M_2	M_1	M_0	Selected Mode
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

$M_2M_1M_0$ Mode Select Bit Definitions

BCD	Operation
0	Hexadecimal Count
1	BCD Count

HEX/BCD Bit Definition

Fig. 6.2 *Control Word Format and Bit Definitions*

Here in the control word format, D0 selects the BCD or binary count while D1, D2, and D3 are used to select one of the modes of operation for the counter which bits D6 and D7 specify. For the operation to take place, the control word is needed to be sent for each separate counter at the same control address register. The identification of the control word of the particular counter is done using bits B6 and B7 of the control word format.

The read/ write operations are performed using bits D4 and D5. Through these bits, the 16-bit count value is read and written in an orderly sequence. Also, each time the read operation will take place the count value is to be read by stopping the counter. Here basically the count value is latched to an internal latch present at the output of each counter before the read operation.

OPERATING MODES OF 8254

Mode 0: Interrupt on terminal count.

Mode 1: Hardware Retriggerable One-Shot.

Mode 2: Rate Generator.

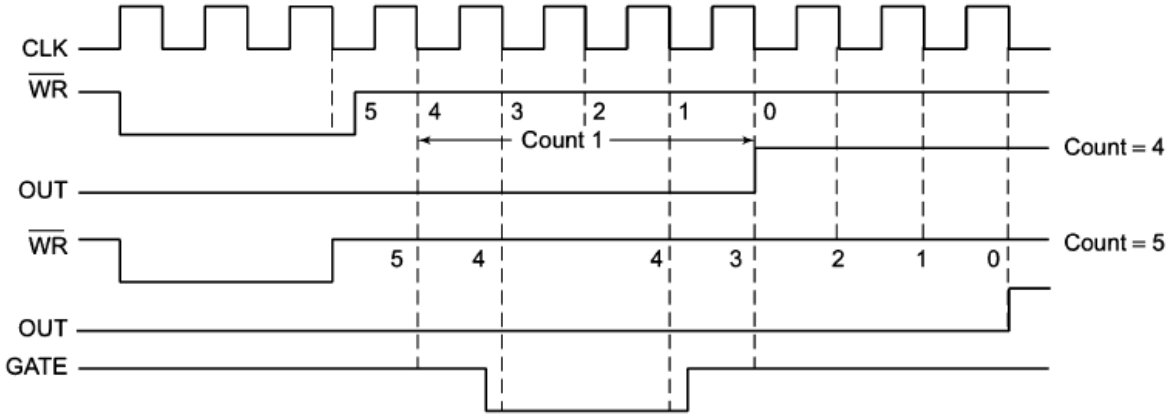
Mode 3: Square Wave Mode.

Mode 4: Software Triggered Mode.

Mode 5: Hardware Triggered Mode.

MODE 0 (Interrupt on terminal count.)

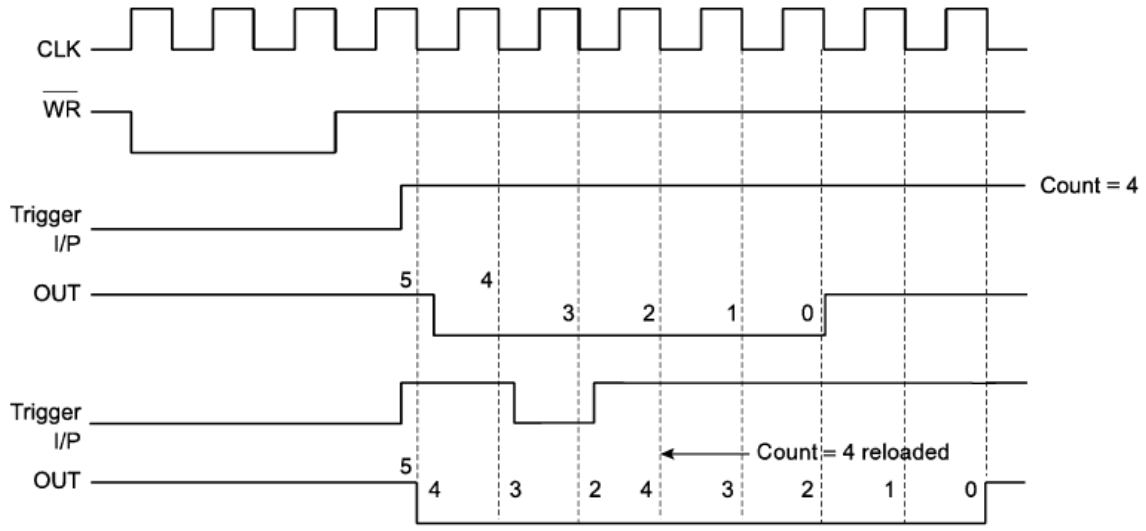
- Mode 0 is typically used for event counting
- After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.
- After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N +1 CLK pulses after the initial count is written.
- GATE =1 enables counting; GATE = 0 disables counting.
- GATE has no effect on OUT. If G becomes a logic 0 in the middle of the count, the counter will remain stop until G again becomes a logic 1.
- If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count.



Waveforms of $\overline{WR}$, OUT and GATE in Mode 0

MODE 1 (Programmable monoshot)

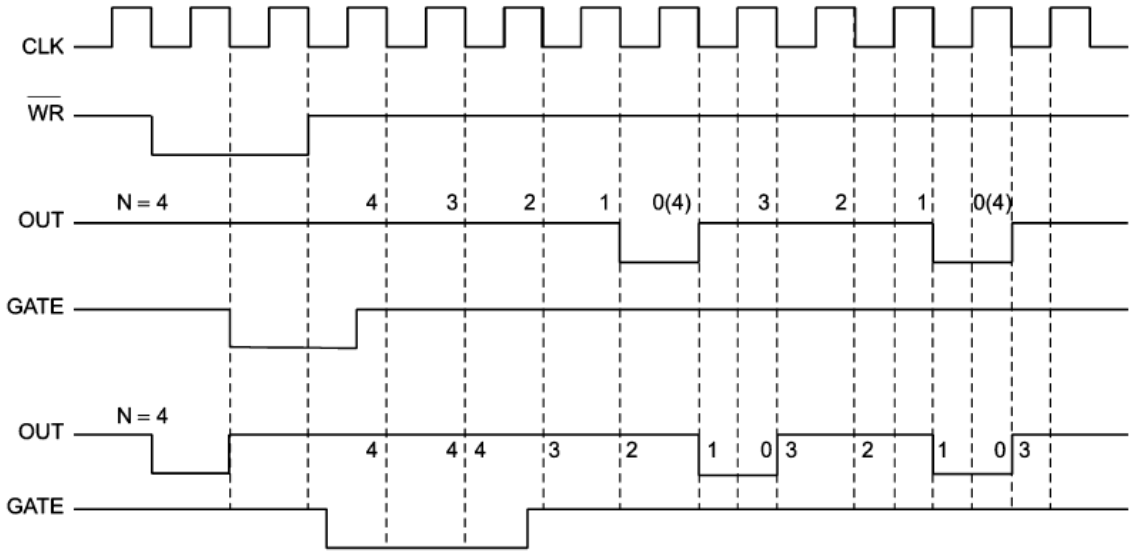
- Causes the counter to function as a retriggerable, monostable multivibrator (one-shot).
- OUT is initially (after loading CW) high. Also remain high when count is written.
- When gate is triggered, OUT goes low and will remain low until the Counter reaches zero. On completion of count OUT goes high again
- If the GATE input occurs within the duration of counting, the counter is again reloaded with the count and start counting from the beginning.



WR, GATE and OUT Waveforms for Mode 1

MODE 2 (RATE GENERATOR)

- It is also called **divide by N counter**
- Allows the counter to generate a series of continuous pulses that are one clock pulse wide.
- The separation between pulses is determined by the count.
- If count N is reloaded then, output will remain high for (N-1) clock period and low for 1 clock period
- For example, for a count of 4, the output is a logic 1 for 3 clock period and low for 1 clock period. This cycle is repeated until the counter is programmed with a new count or until G pin is placed at a logic 0 level.
- The output is normally high after initialization or even a low signal on GATE input can force the output to go high.
- If the GATE goes high, the counter starts counting down from the initial value



Waveforms at Pin WR and OUT In Mode 2

MODE 3 (Square Wave Generator)

- Generates a continuous square wave at the out connection.ie, **Square wave Generator**
- Mode 3 is similar to Mode 2 except for the duty cycle of OUT.
- If the count (N) is even, the output is high for one half (N/2) of the count and low for one half (N/2) of the count.
- If the count (N) is odd, the output is high for one clocking period longer than it is low i.e. high for (N+1)/2 clock pulses and low for (N-1)/2 clock pulses
- For example, if the count is programmed for a count of 5, the output is high for three clocks and low for two clocks.
- Gate should be maintained at logic 1 always (GATE =1 enables counting; GATE =0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required).

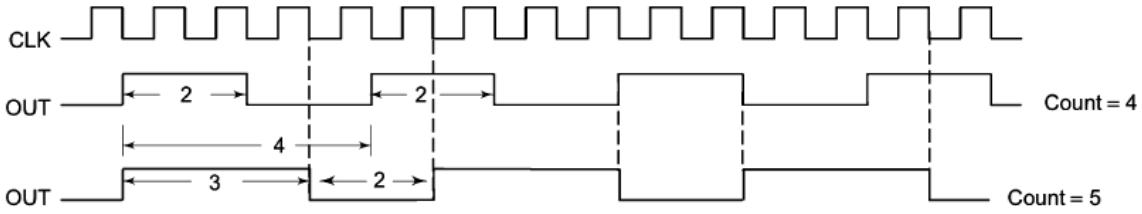
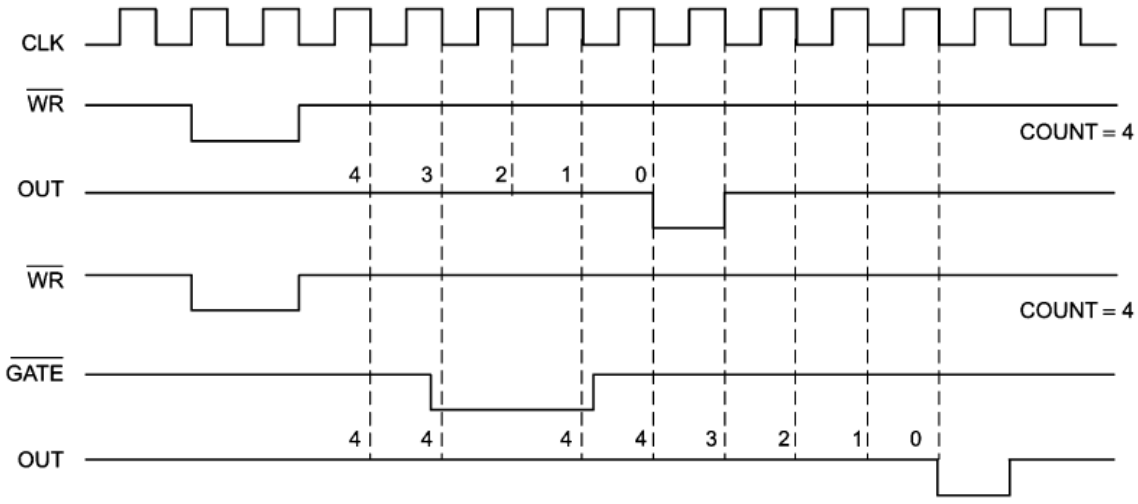


Fig. 6.6 *Waveforms for Mode 3*

MODE 4 (Software Triggered One-shot)

- Allows the counter to produce a single pulse at the output.
- If count of N is loaded, then OUT will be high for N clock cycles and low for one clock cycle at the end.
- The cycle does not begin until the counter is loaded again.
- G input must be maintained at logic 1 throughout the operation.
- This mode operates as a software triggered one-shot.

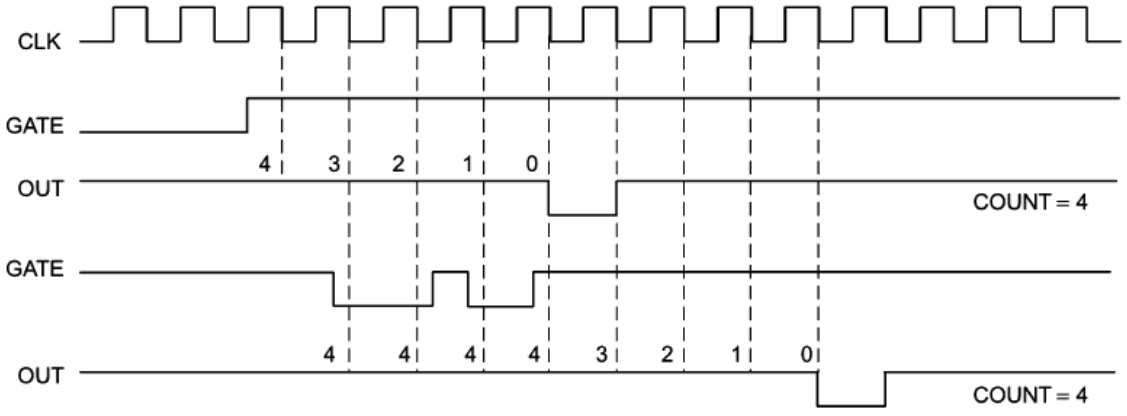


$\overline{WR}$, GATE and OUT Waveforms for Mode 4

MODE 5 (Hardware Triggered Mode)

- A hardware triggered one-shot that function as mode 4, except that it is started by a trigger pulse on the G pin instead of by software.

- When the GATE pulse is triggered from low to high the count begins. At the end of the count OUT goes low for one clock period.
- This mode is also called HARDWARE TRIGGERED STROBE (RETRIGGERABLE)



Waveforms in Mode 5

REVIEW QUESTIONS

1. Explain the block diagram of 8254, programmable interval timer.
2. Explain the architecture and modes of operation of 8254 programmable Timer/ Counter with necessary diagrams.